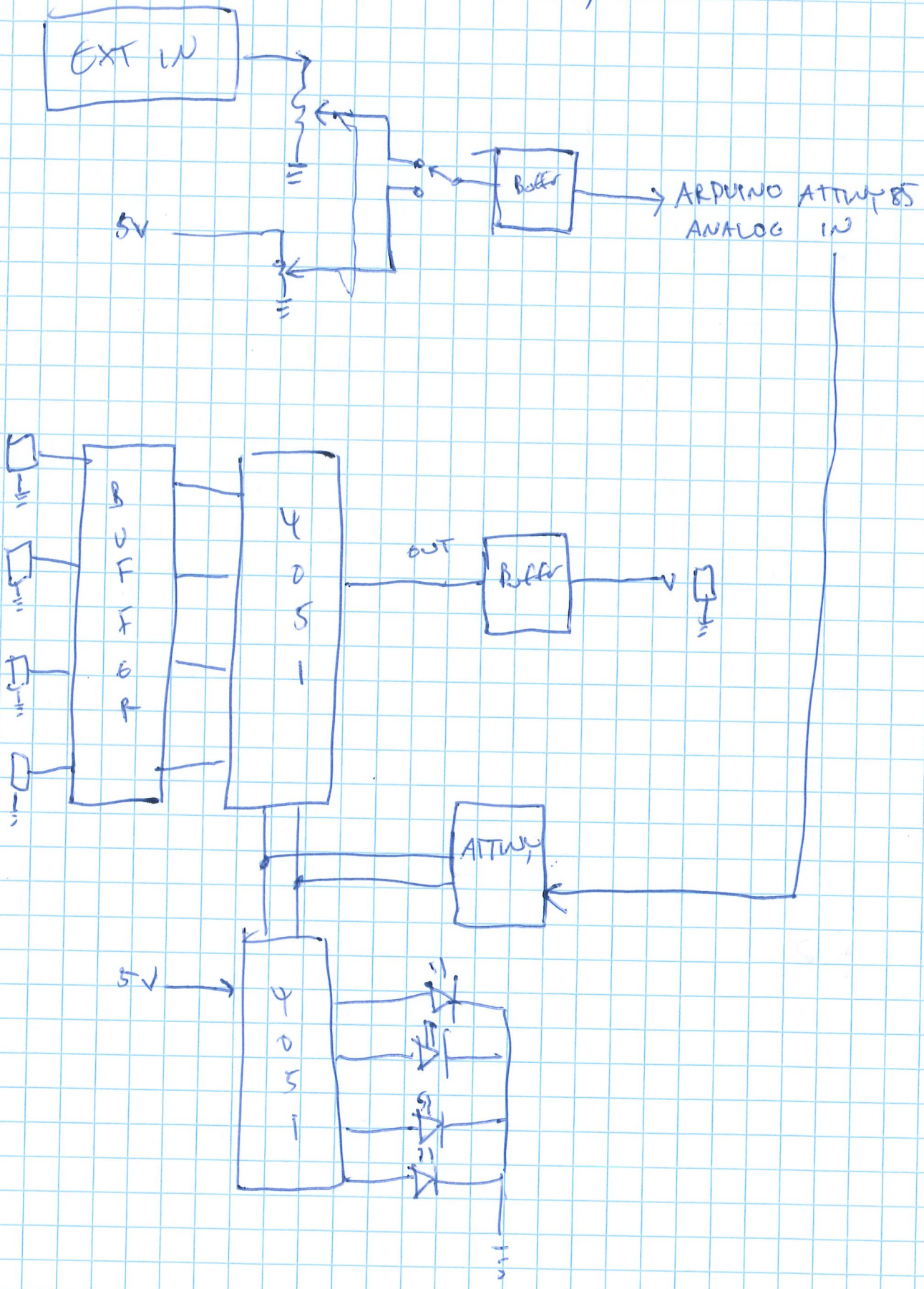
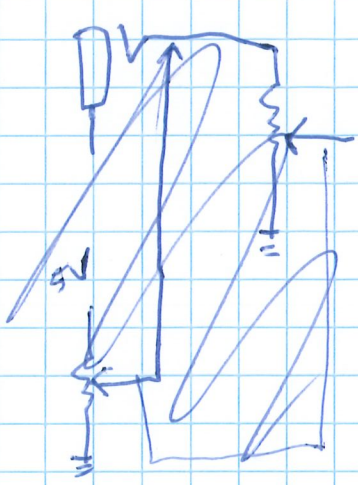
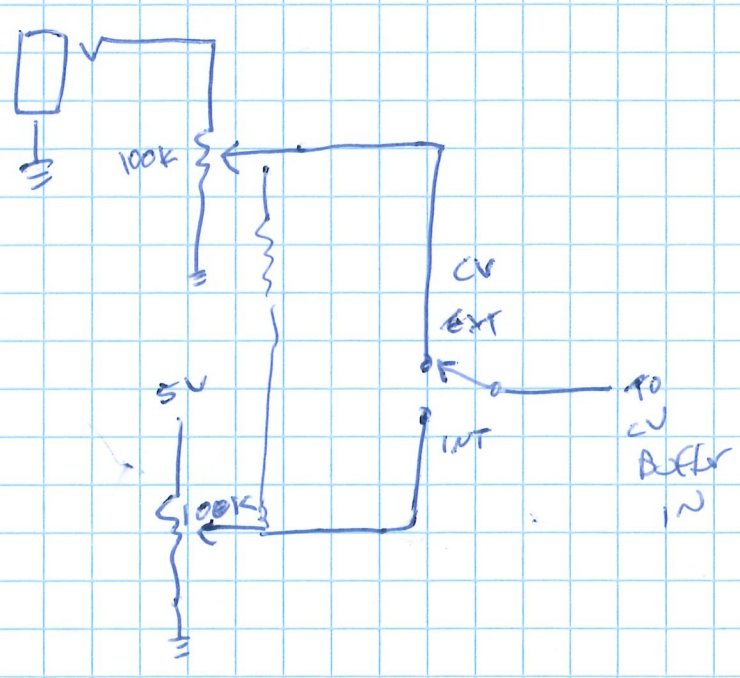
4051 SWITCH

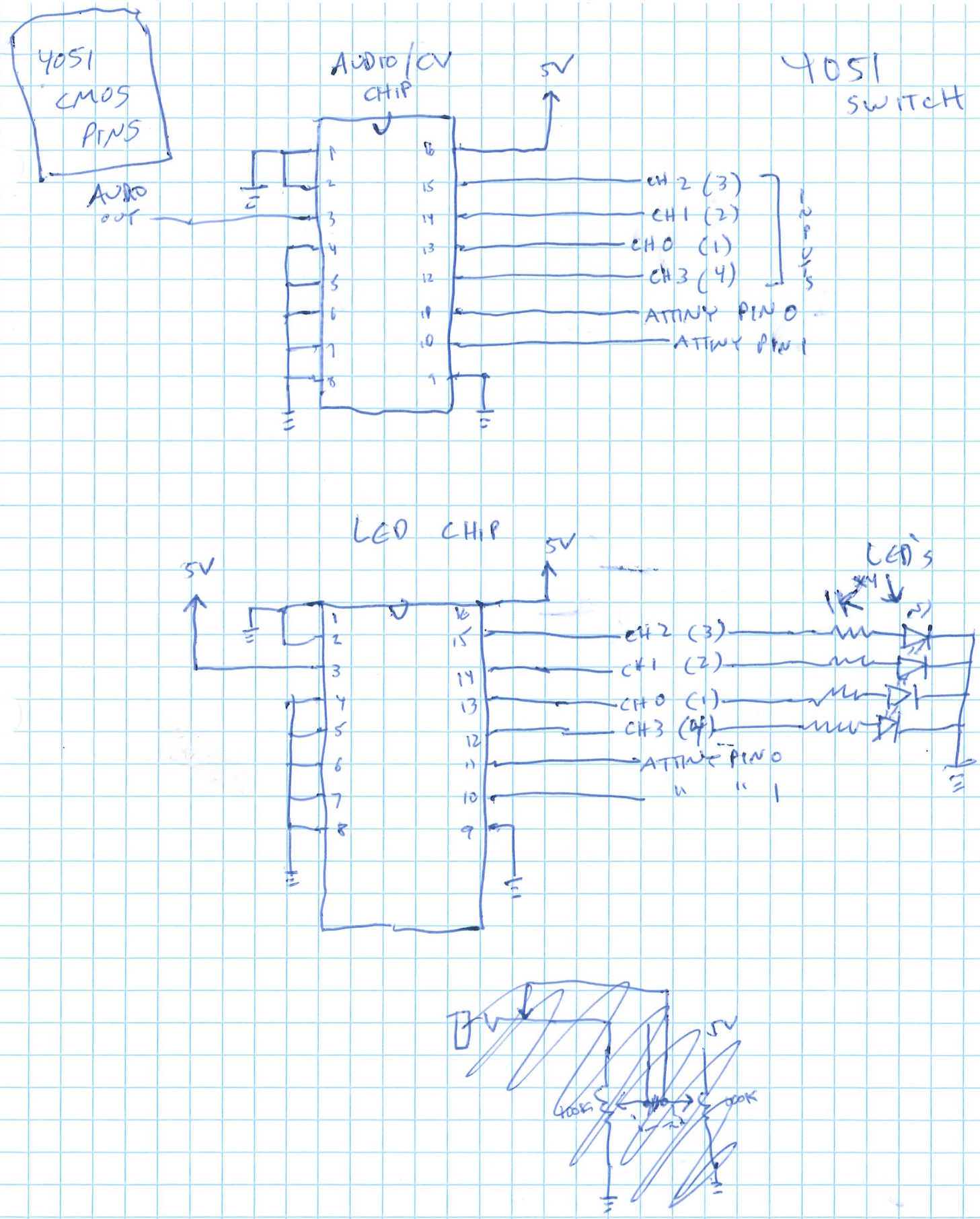
Block diagram

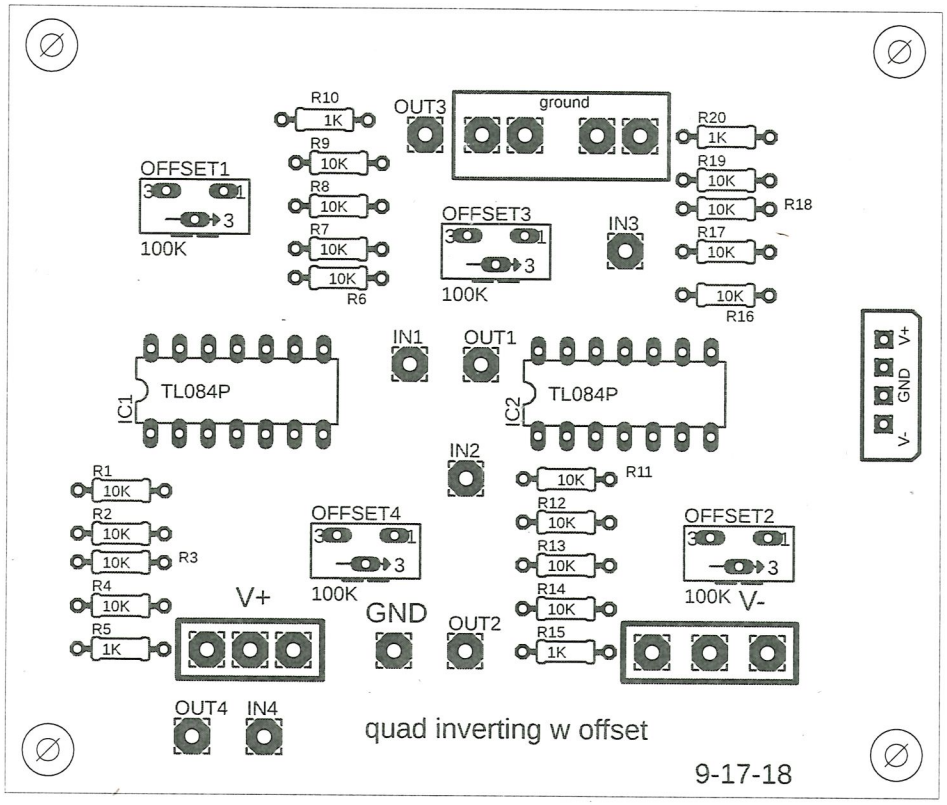


4051 INPUT/VOLUME POT

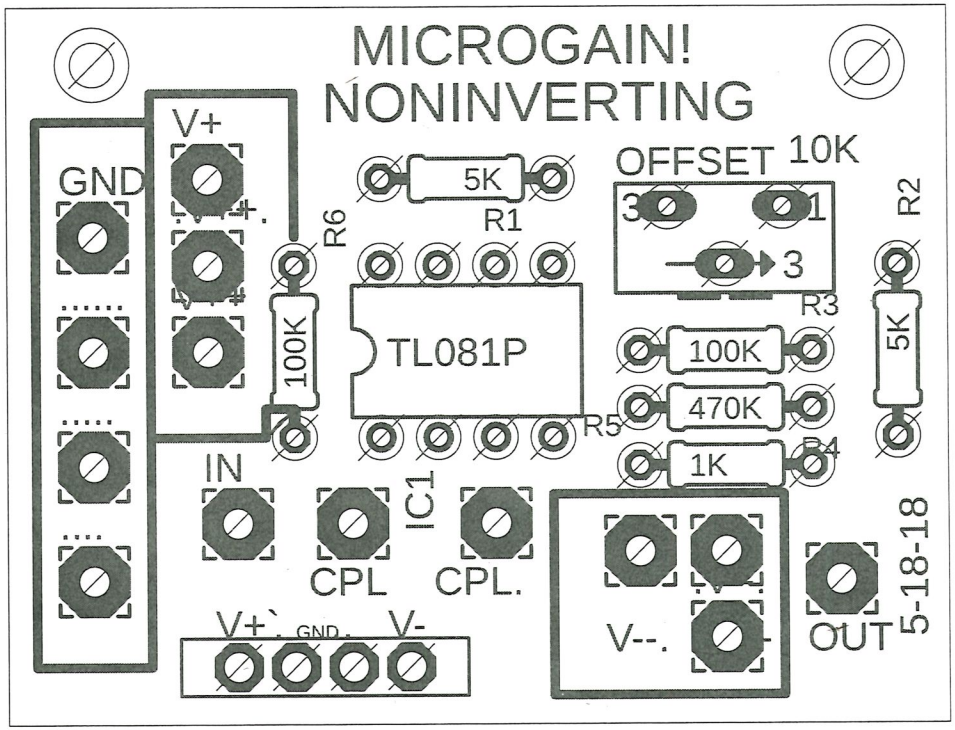




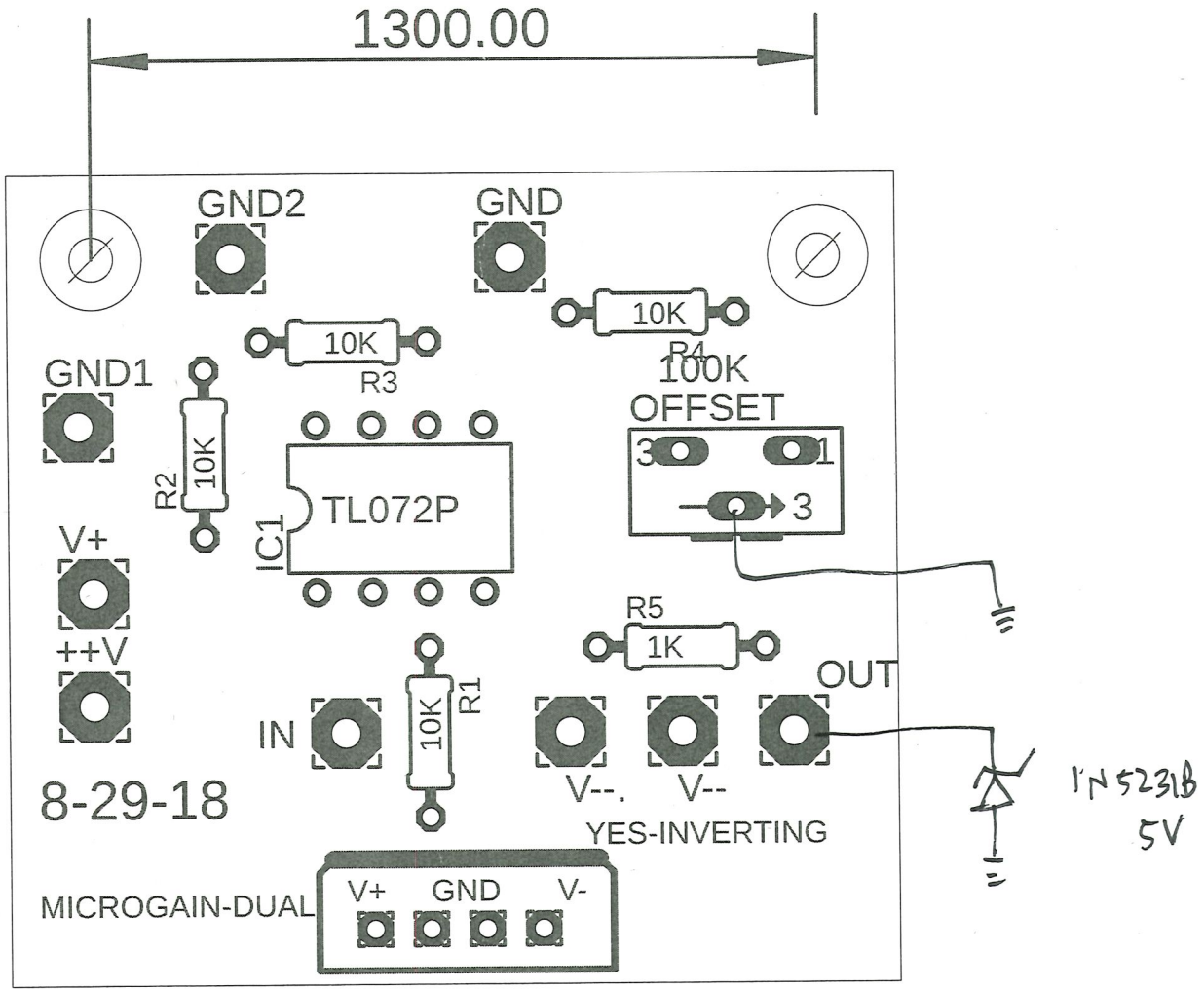

4051 CMOS PINS
AUDIO OUT
AUDIO/CV CHIP
5V
4051 SWITCH
CH 2 (3)
CH 1 (2)
CH 0 (1)
CH 3 (4)
INPUTS
ATTINY PIN 0
ATTINY PIN 1
LED CHIP
5V
LED'S
CH 2 (3)
CH 1 (2)
CH 0 (1)
CH 3 (4)
ATTINY PIN 0
" " 1
5V
100K
100K


R10
1K
OUT3
ground
R20
1K
R9
10K
R19
10K
OFFSET1
R8
10K
10K
R18
R7
10K
OFFSET3
IN3
R17
10K
100K
10K
R6
100K
10K
R16
IN1
OUT1
V+
GND
V-
IC1
TL084P
IC2
TL084P
IN2
R1
10K
10K
R11
R2
10K
R12
10K
OFFSET2
R3
R13
10K
OFFSET4
3
1
R4
10K
R14
10K
100K
V+
GND
OUT2
100K
V-
R5
1K
R15
1K
OUT4
IN4
quad inverting w offset
9-17-18

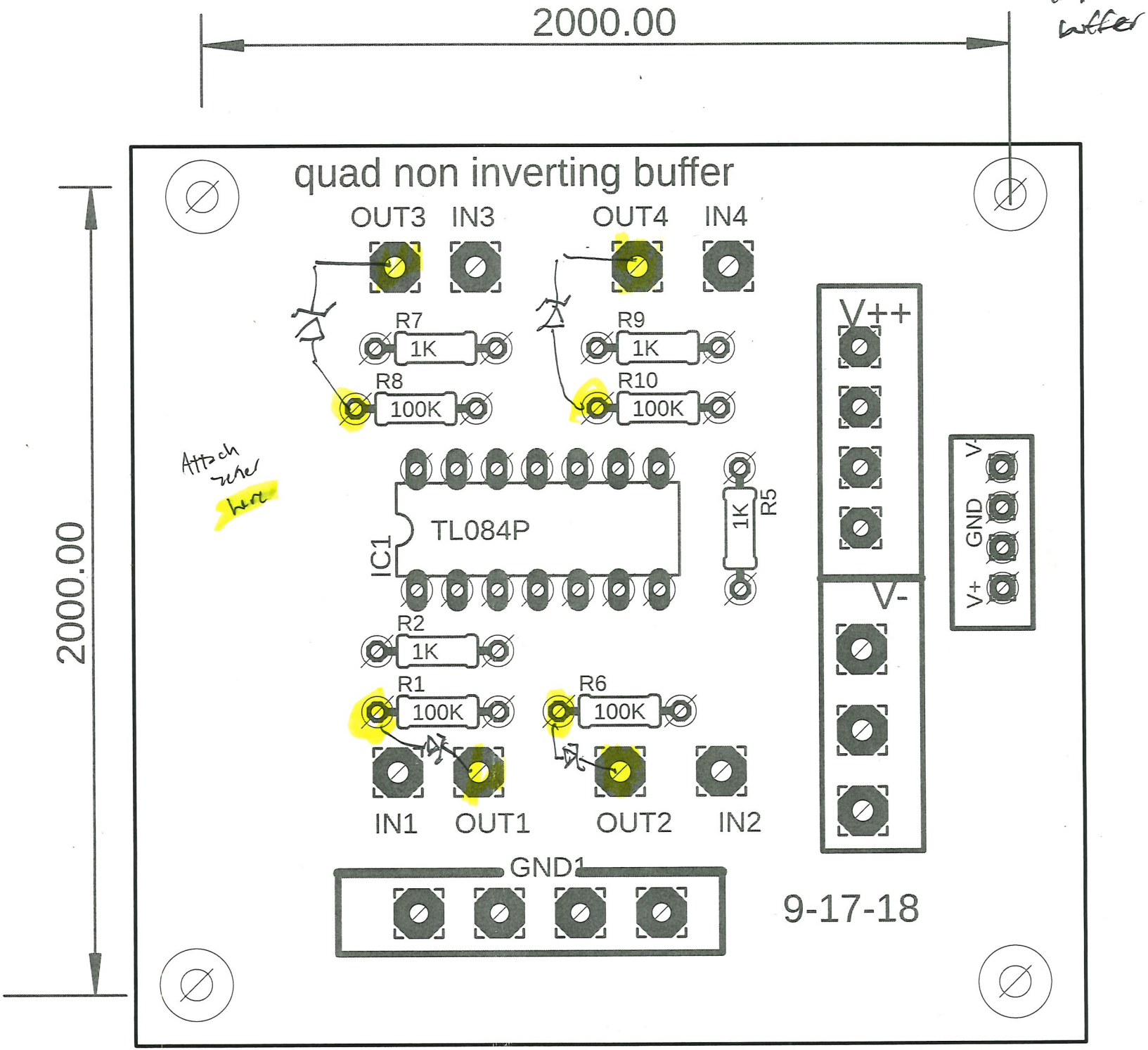
4051 switch
output Buffer



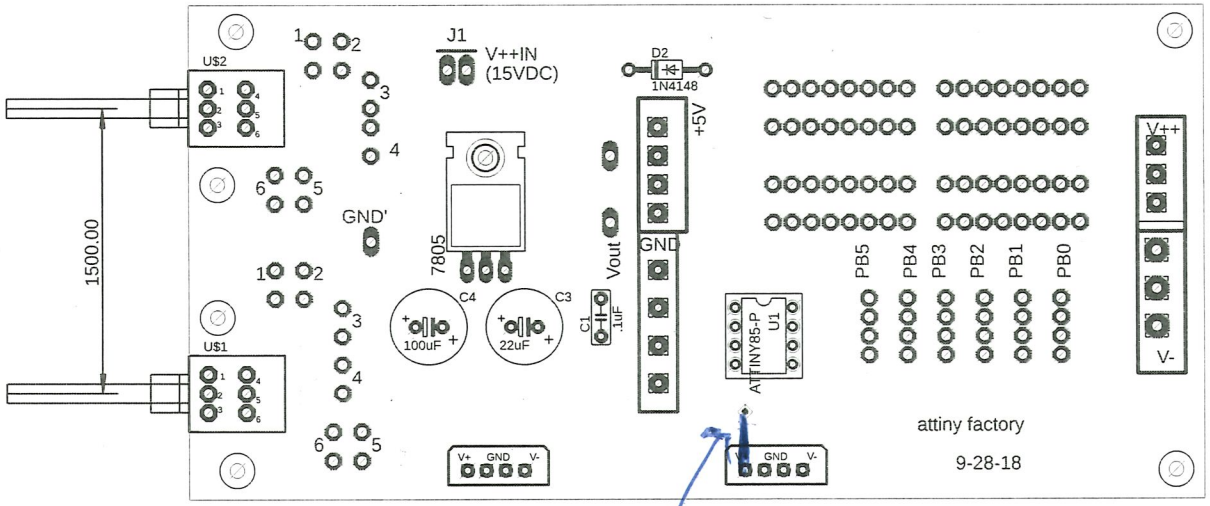
4051 Switch
CV INPUT
Buffer



4051B switched input buffer



ATTINY Factory Rev 1

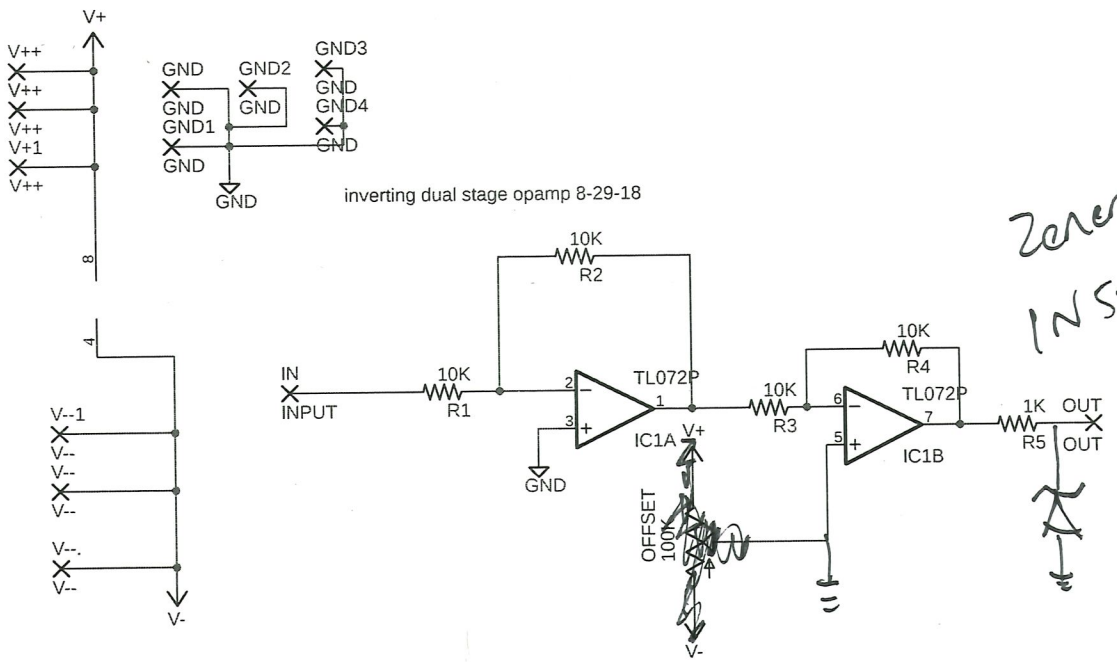


FIX

a) cut this trace

b) solder V+ to 15V rail using kludge wire

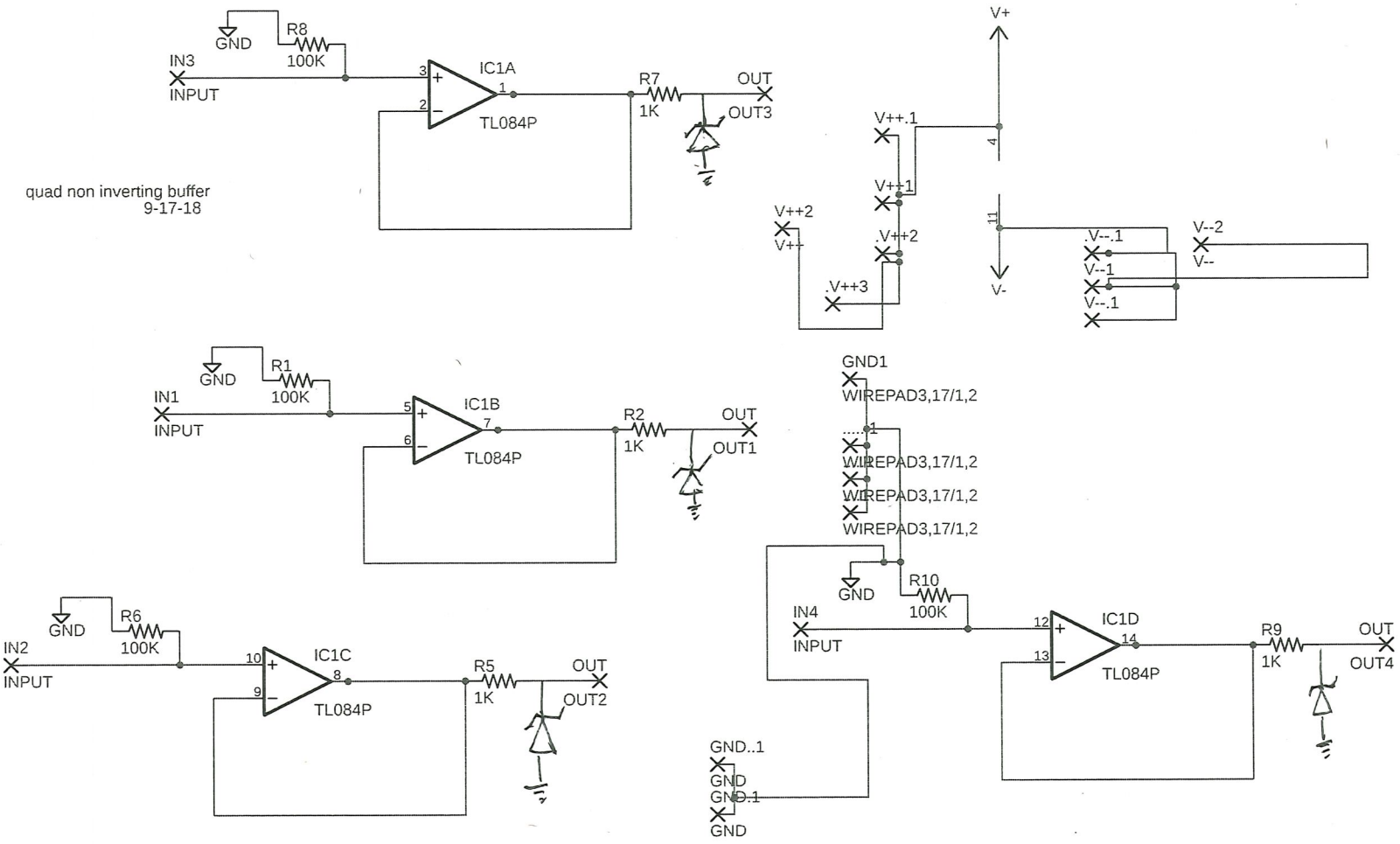
4051 Switch
CV input buffer
5



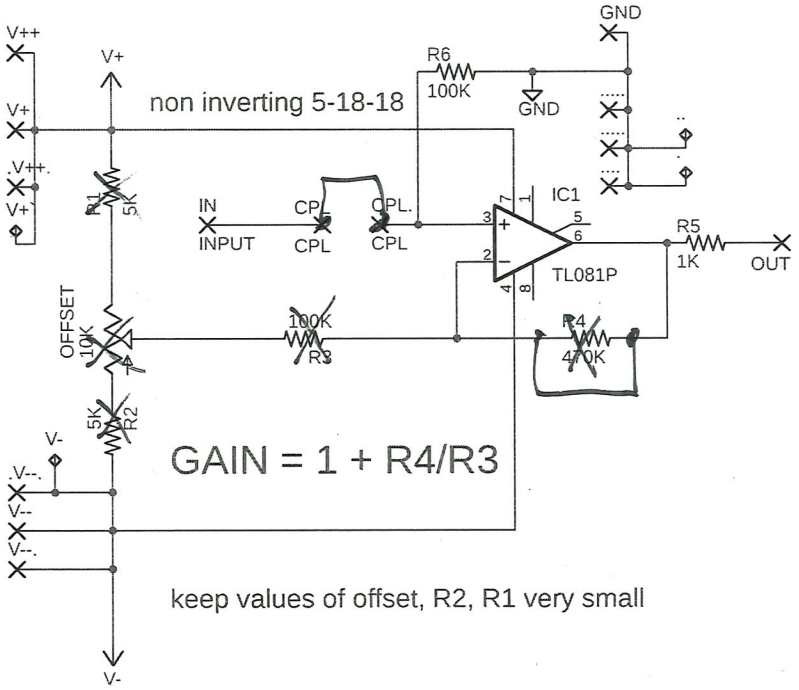
Zener = 5V
1N5231B

4051 switch
input buffer

All zero 5V = LM5231B

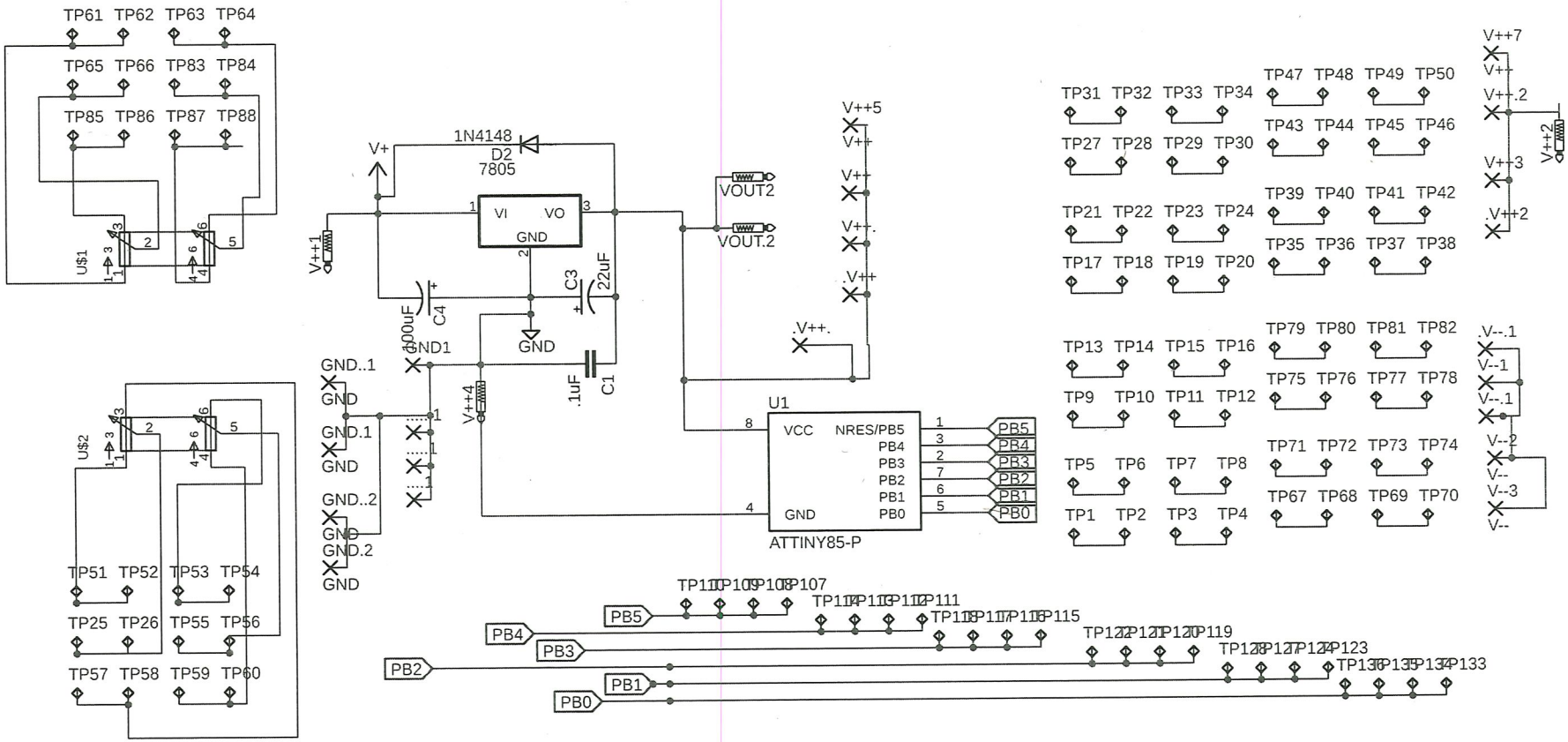


4051 switch
output buffer



jump CPL
jumpR4
use R5

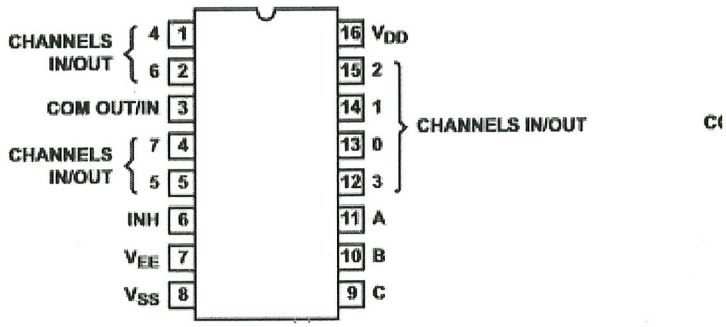
ATTINY FACTORY
Rev 1 schematic



What you have to know about 4051.

5 Pin Configuration and Functions

CD4051B E, M, NS, and PW Package
16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP
(Top View)



CD4052B E, M, NS, and P

End of the data sheet.

Functional Diagrams of CD405xB

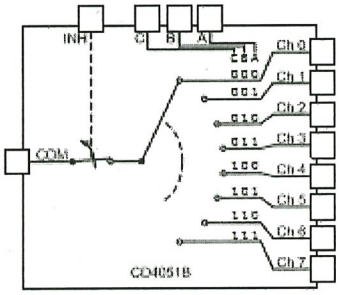


Table 1. Truth Table[1]

INPUT STATES				ON CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				

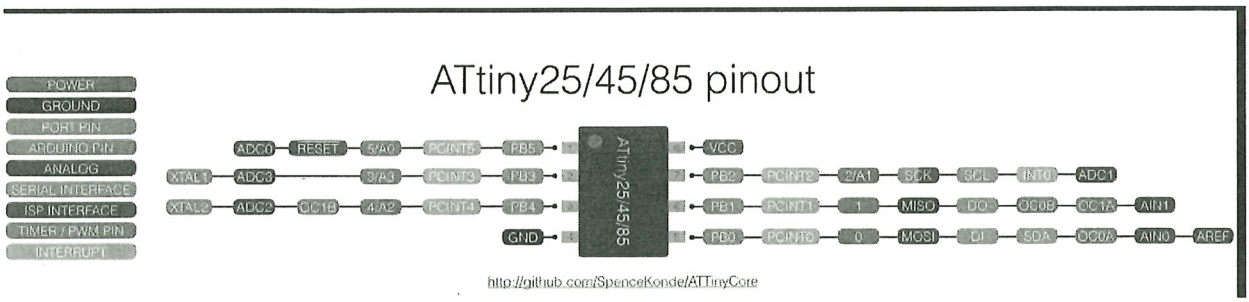
What you have to know about 4051

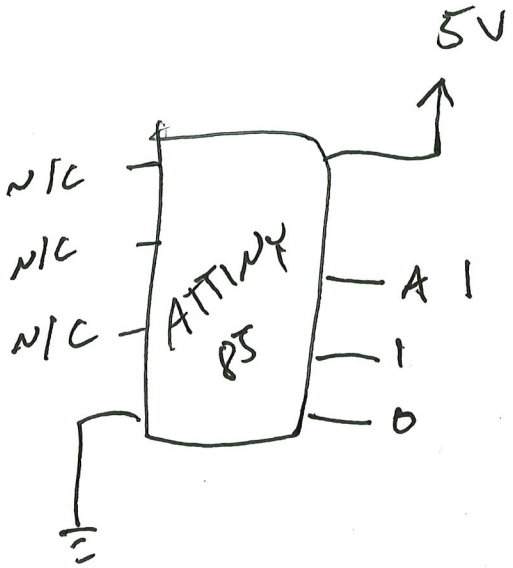
4051 need to know page 2

Pin Functions CD4051B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See Table 1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See Table 1.
10	B	I	Channel select B. See Table 1.
11	A	I	Channel select A. See Table 1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V_{DD}	—	Positive power input

4051 switch


ATtiny25/45/85 pinout
POWER
GROUND
PORT PIN
ARDUINO PIN
ANALOG
SERIAL INTERFACE
ISP INTERFACE
TIMER / PWM PIN
INTERRUPT
ADC0 RESET 5/A0 PCINT5 PB5
XTAL1 ADC3 3/A3 PCINT3 PB3
XTAL2 ADC2 OC1B 4/A2 PCINT4 PB4
GND
ATtiny25/45/85
VCC
PB2 PCINT2 2/A1 SCK SCL INT0 ADC1
PB1 PCINT1 1 MISO DO OC0B OC1A AIN1
PB0 PCINT0 0 MOSI DI SDA OC0A AIN0 AREF
http://github.com/SpenceKonde/ATTinyCore


5V
N/C
N/C
N/C
ATTINY
85
A 1
1
0